Amendments to the Claims:

Please add new claims 17-20 as follows. Please amend claim 1, 9, and 14 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor memory integrated circuit, comprising:

a plurality of first data IO pads, a plurality of address and instruction pads, and a plurality of second data IO/address pads, which are arranged in groups adjacent each other,

wherein the plurality of first data IO pads are adjacent to a first side of the plurality of the address and instruction pads and the plurality of second data IO/address pads are adjacent to a second side of the plurality of address and instruction pads opposite the first side, and wherein each of the plurality of the second data IO/address pads is used as a second data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form.

2. (Previously Presented) The circuit of claim 1, further comprising, for each of the plurality of second data IO/address pads:

a data input/address buffer connected to the second data IO/address pad to buffer data IO/address signals applied to the second data IO/address pad;

a data input latch that is enabled in response to a first state of the control signal to latch and output data signals buffered by the data input/address buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output address signals buffered by the data input/address buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

3. (Original) The circuit of claim 1, wherein the first package form is a BGA package.

4. (Original) The circuit of claim 1, wherein the second package form is a TSOP package.

5. (Withdrawn) A semiconductor memory integrated circuit, comprising:

a plurality of first data IO pads, a plurality of address and instruction pads, and a plurality of second data IO/address and instruction pads, which are arranged in groups adjacent each other,

wherein each of the plurality of the second data IO/address and instruction pads is used as a second data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form.

6. (Withdrawn) The circuit of claim 5, further comprising,

The circuit of claim 1, further comprising, for each of the plurality of second data IO/address and instruction pads:

a data input/address and instruction buffer connected to the second data IO/address and instruction pads to buffer data IO/address and instruction signals applied to the second data IO/address and instruction pads;

a data input latch that is enabled in response to a first state of the control signal to latch and output data signals buffered by the data input/address and instruction buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output address and instruction signals buffered by the data input/address and instruction buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

7. (Withdrawn) The circuit of claim 5, wherein the first package form is a BGA package.

8. (Withdrawn) The circuit of claim 5, wherein the second package form is a TSOP package.

9. (Currently Amended) A semiconductor memory integrated circuit, comprising:

a plurality of data IO pads, a plurality of address and instruction pads, and a plurality of generic pads, which are arranged in groups adjacent each other,

wherein the plurality of data IO pads are adjacent to a first side of the plurality of the address and instruction pads and the plurality of generic pads are adjacent to a second side of the plurality of address and instruction pads opposite the first side, and wherein each of the plurality of generic pads is used as a data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form.

10. (Previously Presented) The circuit of claim 9, further comprising, for each of the plurality of the generic pads:

a data input/address buffer connected to the generic pad to buffer a data IO/address signal applied to the generic pad;

a data input latch that is enabled in response to a first state of the control signal to latch and output a data signal buffered by the data input/address buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output an address signal buffered by the data input/address buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

11. (Previously Presented) The circuit of claim 9, wherein the first package form is a BGA package.

12. (Previously Presented) The circuit of claim 9, wherein the second package form is a TSOP package.

13. (Previously Presented) A semiconductor memory integrated circuit, comprising:

a plurality of data IO pads, a plurality of address and instruction pads, and a plurality of generic pads, which are arranged in groups adjacent each other,

wherein each of the plurality of the generic pads is used as a data IO pad in response to a control signal when packaged into a first package form and is used as an address or instruction pad in response to the control signal when packaged into a second package form.

14. (Currently Amended) The circuit of claim 13, further comprising, for each of the plurality of the generic pads:

a data input/address [[or]]and instruction buffer connected to the ~~second data IO/address or instruction pads~~ generic pad to buffer data IO/address [[or]]and instruction signals applied to the ~~second data IO/address or instruction~~ generic pad;

a data input latch that is enabled in response to a first state of the control signal to latch and output a data signal buffered by the data input/address and instruction buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output an address and instruction signal buffered by the data input/address and instruction buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

15. (Previously Presented) The circuit of claim 13, wherein the first package form is a BGA package.

16. (Previously Presented) The circuit of claim 13, wherein the second package form is a TSOP package.

17. (New) A semiconductor memory integrated circuit, comprising:

a plurality of first data IO pads, a plurality of address and instruction pads, and a plurality of second data IO/address pads, which are arranged in groups adjacent each other,

wherein each of the plurality of the second data IO/address pads is used as a second data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form, the circuit further comprising, for each of the plurality of second data IO/address pads:

a data input/address buffer connected to the second data IO/address pad to buffer data IO/address signals applied to the second data IO/address pad;

a data input latch that is enabled in response to a first state of the control signal to latch and output data signals buffered by the data input/address buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output address signals buffered by the data input/address buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

18. (New) The circuit of claim 17, wherein the first package form is a BGA package and the second package form is a TSOP package.

19. (New) A semiconductor memory integrated circuit, comprising:

a plurality of data IO pads, a plurality of address and instruction pads, and a plurality of generic pads, which are arranged in groups adjacent each other,

wherein each of the plurality of generic pads is used as a data IO pad in response to a control signal when packaged into a first package form and is used as an address pad in response to the control signal when packaged into a second package form, the circuit further comprising, for each of the plurality of the generic pads:

a data input/address buffer connected to the generic pad to buffer a data IO/address signal applied to the generic pad;

a data input latch that is enabled in response to a first state of the control signal to latch and output a data signal buffered by the data input/address buffer;

an address input latch that is enabled in response to a second state of the control signal to latch and output an address signal buffered by the data input/address buffer;

a data output latch that is enabled in response to the first state of the control signal to latch and output internally generated data; and

a data output buffer that is enabled in response to the second state of the control signal to buffer data output by the data output latch.

20. (New) The circuit of claim 19, wherein the first package form is a BGA package and the second package form is a TSOP package.